IN THE CLAIMS

1-23. Canceled

24. (Currently amended) An apparatus for use in a transmitter comprising:

a variable gain amplifier, the variable gain amplifier including:

an inductively loaded folded cascode circuit that inputs an input differential signal having a Voltage Drain-Drain (VDD) [[VDD]]-referenced output level and outputs a current;

an input current load circuit that inputs the current from the inductively-loaded folded cascode circuit and outputs an output differential signal having a ground-referenced output level;

a plurality of gain cells, each gain cell coupled to the input current load circuit and receiving the output differential signal, each gain cell comprising two current mirror circuits; and

a plurality of switching circuits, each switching circuit coupled to one of the plurality of gain cells and each switching circuit operating in a positive mode and in a negative mode, the negative mode having an opposite polarity of the positive mode, and wherein the plurality of switching circuits operate to place more of the plurality of gain cells in the positive mode than in the negative mode.

25. (Original) The apparatus according to claim 24 wherein the positive mode and the negative mode occur at the same time in a gain cell of the variable gain amplifier, thereby providing for fine gain adjustments.

26. (Currently amended) The apparatus according to claim 24 wherein the input current load circuit is comprised of four n-type metal-oxide-semiconductor (NMOS) ~~NMOS~~ transistors arranged in a cascode configuration.

27. (Original) The apparatus according to claim 26 wherein the input current load circuit is mirrored by each of the plurality of gain cells.

28. (Original) The apparatus according to claim 27 wherein each of the current mirror circuits in each of the plurality of gain cells comprises three NMOS transistors.

29. (Currently amended) The apparatus according to claim 28 wherein each of the plurality of switching circuits includes an NMOS and a p-type metal-oxide-semiconductor (PMOS) ~~PMOS~~ transistor that operate to create the positive mode and an NMOS and a PMOS transistor that operate to create the negative mode.

30. (Original) The apparatus according to claim 24 wherein the input current load circuit is mirrored by each of the plurality of gain cells.

31. (Original) The apparatus according to claim 24 wherein each of the current mirror circuits in each of the plurality of gain cells comprises three NMOS transistors.

32. (Original) The apparatus according to claim 24 wherein each of the plurality of switching circuits includes an NMOS and a PMOS transistor that operate to create the positive mode and an NMOS and a PMOS transistor that operate to create the negative mode.

33. (Original) The apparatus according to claim 24 further comprising:

an intermediate frequency upmixer having an intermediate frequency upmixer output coupled to an input of the variable gain amplifier; and

a radio frequency upmixer having a radio frequency upmixer input to an output of the variable gain amplifier.

34. (New) The apparatus according to claim 24 wherein the input current load circuit is commonly connected to each gain cell and the gain cells have inputs for receiving the output differential signal, the inputs of each gain cell being commonly connected to the output differential signal.

35. (New) The apparatus according to claim 24 wherein the switching circuits operate to place a selected portion of the plurality of gain cells in the positive mode, the portion being selected to maintain a preferred output power level.